Standard Gate-Driver Optocouplers

AN-3009/D

HOW DOES A STANDARD GATE−DRIVER OPTOCOUPLER WORK?

The FOD31xx family of gate drivers functions as a power buffer to control the gate of a power MOSFET or IGBT. It is designed to supply the peak charging current required by the MOSFET or IGBT's gate input to turn the device ON. It does this by providing a positive voltage (V_{OH}) to the power semiconductor's gate. Turning the MOSFET or IGBT OFF is accomplished by pulling the gate of the driven device to zero voltage (V_{OL}) or lower.

Many power control applications use a "totem pole" high− and low−side connection of two or more series−connected power semiconductors. The high−side N−channel MOSFET drain is connected to a positive (+) terminal of a supply and its source is connected to the drain of the low−side transistor. The source of the low−side transistor is connected to the negative (−) side of the system supply. One side of the driven load is connected at the common node of the high−side and low−side transistors. Proper control of the high−side and low−side transistors requires that neither transistor is ON or conducting at the same time. The current through these series high−side and low−side devices is called "shoot−through" current. Shoot−through current wastes power and can cause damage to the high− and low−side transistors.

The most common technique to eliminate shoot−through current is to add a delay or hold−off time between switching on the high−side or low−side switch. The delay is introduced by controlling the timing of the signal supplied to the high−side and low−side gate drivers.

Figure 1 shows the gate drive internal block diagram. Each section of the driver is supplied by a common power or bias source. At initial power turn−on, there are circuit delays due to the circuit's complexity. This complexity can introduce (during initial power−up) a situation where the gate's output follows the rising edge of the applied V_{DD} supply until the supplies have stabilized. Once the bias levels are correct, the gate drive output returns to its correct state, controlled by the LED.

This application note discusses the key design criteria, including LED driving, initial conditions, maximum switching frequency, and power.

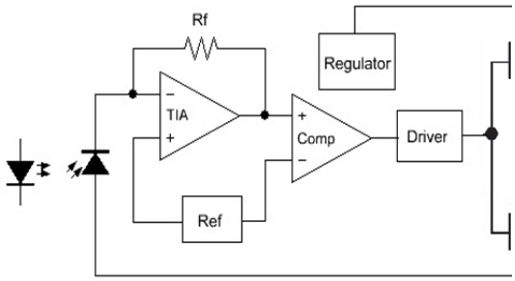

Figure 1. FOD31xx Block Diagram

INITIAL CONDITIONS: DEVICE STARTUP

Operational Conditions

There are three power supplies in a typical inverter application. The first is a logic supply (+3.3 V or +5 V or +10 V). The second is an isolated low and high side driver supply (+20 V FOD3182, +25 V FOD3120). The third is a high−voltage supply to power the MOSFETs / IGBTs. To minimize any impact of the bias supply stabilization time, one solution is to control the sequence of power supply activation:

- First: logic supply − initial condition, LED current = 0 mA, LED OFF.
- Second: isolated low− and high−side driver supply, $V_O = V_G = 0$ V, power MOSFETs OFF.
- Third: high−voltage supply to power MOSFETS.

The turn−on sequence delay should accommodate power−on reset for logic control and bootstrap charge time for the driver isolated supply.

LED Drive

The peak forward current, $I_{F(peak)}$, is <1 A (1 μs, 300 pps). The recommended operational current is 10 mA to 16 mA. The rate of current rise is less than 250 ns. The fast rate of LED−current rise minimizes propagation delay and output switching jitter.

Power Supply Considerations

The FOD31xx products are high−gain (23 db), high−power−output, optical amplifiers. They require a power supply with a low output impedance over the range of DC to 40 MHz. Using low−ESR bypass capacitors and a signal ground plane helps minimize self−induced power−supply noise and degraded output rise and fall times.

Propagation Delay on the FOD3182

Figure 2 shows that the propagation delay is independent of the load capacitance and that the typical pulse−width distortion, PWD, is less than 40 ns.

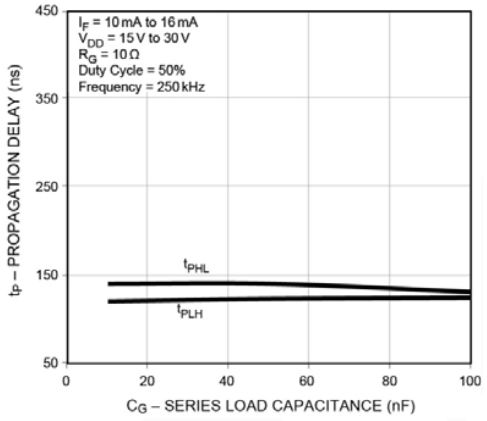

Figure 2. Propagation Delay vs. Series Load Capacitance

Figure 3 shows a propagation delay dependence on LED current. The typical PWD is +4 ns/mA.

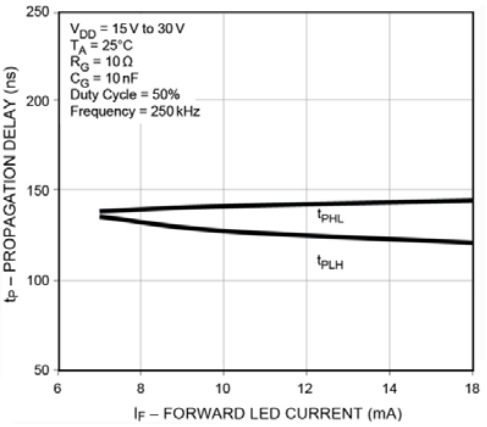

Figure 3. Propagation Delay vs. LED Forward Current

Figure 4 and Figure 5 illustrate independence of delay as a function of series load and supply voltage.

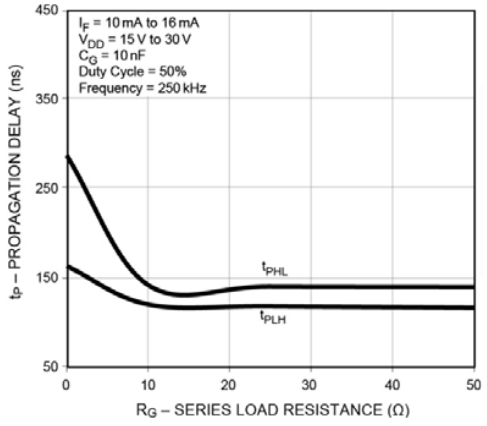

Figure 4. Propagation Delay vs. Series Load Resistance

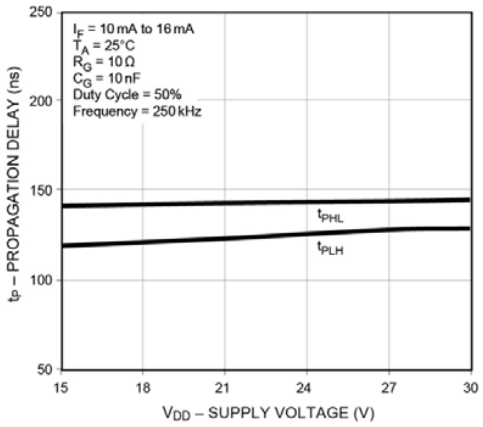

Figure 5. Propagation Delay vs. Supply Voltage

Using a temperature−stable LED and temperature−compensated amplifiers and current sources, the propagation delay changes by, typically, +0.2 ns/°C from −40°C to 100°C, as shown in Figure 6.

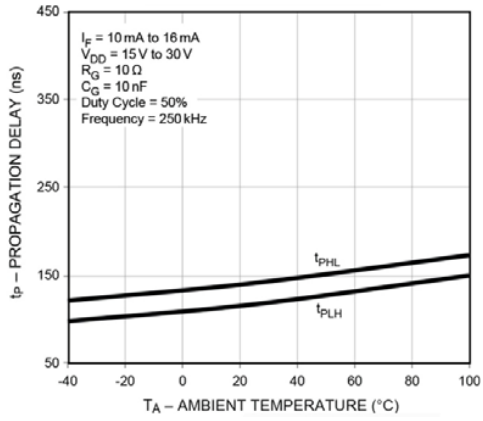

Figure 6. Propagation Delay vs. T_A

The use of a P−channel MOSFET as the pull−up offers two advantages over a bipolar transistor. First, the low $R_{DS(ON)}$ minimizes the internal voltage drop, providing a larger turn−on voltage for a given $V_{CC} - V_{EE}$. Second, the switching delay is smaller than with a multi−stage PNP transistor. Figure 7 shows the voltage drop curve for the FOD3120.

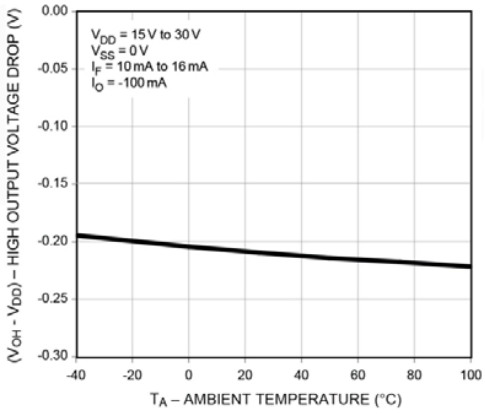

Figure 7. Output High Voltage Drop vs. T_A

GATE DRIVE CMTI (OR NOISE REJECTION) PERFORMANCE

Optically isolated MOSFET and IGBT drivers offer both safety insulation and noise isolation between the load's high voltage and the applications control logic. The FOD31xx family's coplanar construction offers high dielectric insulation and low input to output capacitance, which optimizes safety and minimizes noise coupling. This package construction results in safety compliance for both US and European standards, with working voltage in excess of 800 V.

The interference caused by the electrical noise generated by load switching is blocked through a coplanar optical coupling technique and a special electro−optical shield further reduces the capacitive coupling of the switching transients to the active circuits found in the gate driver.

A typical 240 V_{AC} power converter generates 800 V switching transients with slew rates greater than 6 kV/μs. A transient of this magnitude results in a 3 mA peak current flowing between input and output (when applied to an isolation device with a C_{IO} of only 0.5 pF) *see Figure 8*.

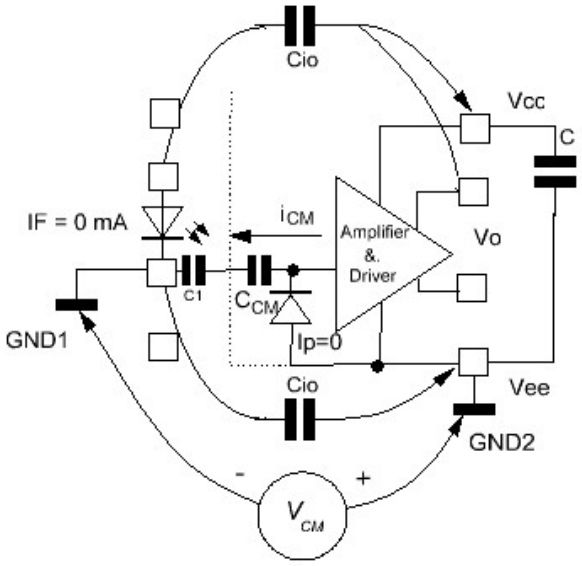

Figure 8. CMTI LED OFF

Figure 8 shows the capacitor that couples the noise current between the input and output of the coupler. In this example, the common−mode transient has a negative rate of voltage swing, as referenced to the coupler's output ground (GND2). This transient draws current from the coupler's output to the input. The package capacitance, C_{IO}, provides the dominant coupling impedance between the input to output. The LED is OFF, thus the output of the gate is in the LOW state. The optical amplifier can be turned ON if sufficient common−mode current, i_{CM}, is drawn out of the input of the amplifier. This noise current, i_{CM}, is quite small given the shield that blocks the effect of the electric field change. This shield results in an effective common−mode coupling capacitance of less than 50 fF. This common−mode shield minimizes coupling into or out of the optical amplifier. The result is that the FOD31xx family rejects +/− common mode transient with peak amplitudes of 1.5 kV and slew rates in excess of 15 kV/μs.

The following summarizes the effects that Common Mode Transients (CMT) have on the FOD31xx family:

- Control current through LED, I_F = 10 mA
  - Output of the driver is HIGH and sourcing current to the load
  - Positive (+) dv/dt pulls current from the amplifier, aiding the photocurrent
  - Negative (−) dv/dt sources current into the amplifier counter, acting on the photocurrent and potentially causing it to transition from HIGH to LOW
- Control current through LED, I_F = 0 mA
  - Output of the driver is LOW and sinking current from the load
  - Positive (+) dv/dt pulls current from the amplifier, potentially causing it to transition from LOW to HIGH
  - Negative (−) dv/dt sources current into the amplifier, helping keep the output in LOW state

Input Common Mode Transient Immunity

Figure 9 and Figure 10 show a half or "H" bridge using two power MOSFETs in a totem−pole configuration. Figure 9 shows the low−side switching, while Figure 10 illustrates high−side switching. Prior to the toggle action, one side is ON and the other OFF. Just before the switching toggle action occurs, both switches are deactivated, creating an OFF dwell or "dead" time.

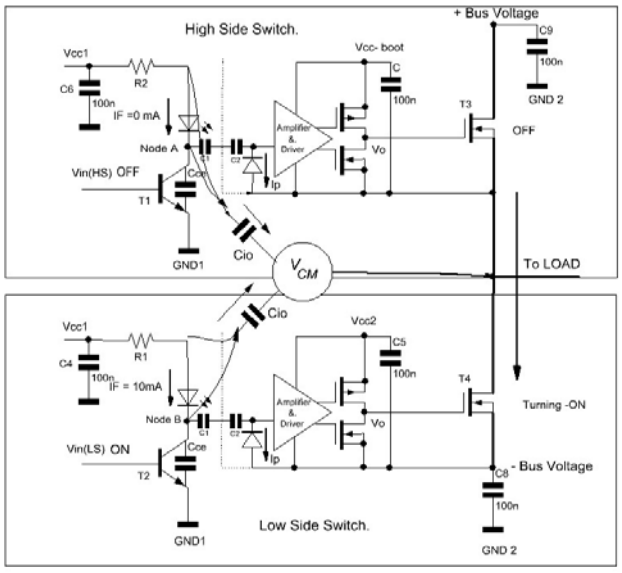

Figure 9. Low−Side ON, High−Side OFF, Negative CMT

Figure 9 shows the CMT being generated as the low−side IGBT is turning ON. This load−switching action creates a negative dv/dt, as seen by both switches of the H−bridge. It is essential that no load shoot−through current occurs during this switching action. Note that input LEDs are connected in

the traditional “series” switching connection. A shoot−through fault can result if the high−side gate drive is momentarily turned ON while the low−side switch is ON. Figure 10 shows the CMT drawing current through the high−side’s LED. The magnitude of the LED current is dependent on: CMT’s dv/dt, assembly input−output parasitic capacitance, and the impedances surrounding the LED. These impedances include the LED current−setting resistor, R2, and the C_{CE} of T1 driving the LED.

An inverter used to generate a 240 V_{AC} power source may create an LED current of 3 mApk with a pulse width of approximately 100 ns. This pulse is sufficient to activate the high−side driver and cause a shoot−through fault. The susceptibility to this fault can be minimized by reducing the off−state impedances surrounding the LED. These lower impedances provide an alternative path for the CMT current caused by the −dv/dt switching action.

The −dv/dt switching action, shown in Figure 9, creates a CMT also seen by the low−side IGBT driver. This transient attempts to draw current through the low−side LED. This transient has minimal effect. The LED is already ON, so forcing more LED current only ensures the correct low−side switching action and the incremental CMT current is shunted to GND1 via transistor T2.

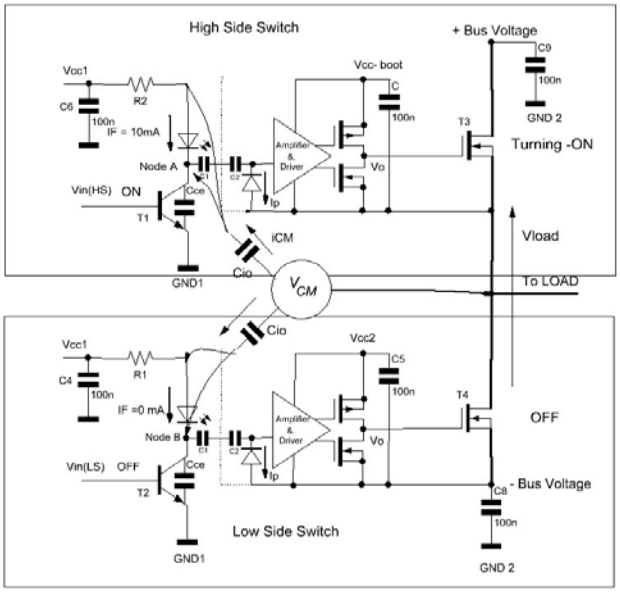

Figure 10. Positive dv/dt − High−Side Switch Turning ON

A positive dv/dt is created when the high−side switch turns ON. Figure 10 shows the effect that this +dv/dt has on the OFF low−side switch. The positive CMT can draw current through the OFF LED in the low−side driver. If the dv/dt is large enough, this CMT can momentarily force the low−side IGBT driver to turn ON. This positive CMT is also seen by the high−side switch. This dv/dt typically helps keep the high−side driver ON.

Minimize Switching CMT with an LED Shunt Drive

CMTI is essential when FOD31xx devices are used in totem−pole half−bridge circuit applications. It is critical that switching transients developed during normal circuit operation do not cause the OFF gate drive to turn ON. This self−induced turn−ON due to half−bridge totem−pole operation creates the need for an LED shunt drive to improve operational noise immunity.

In the previous example, the LEDs were connected in the traditional “series” drive configuration. The CMT can sink or source current through the package, C_{IO}, causing the OFF LED to conduct. The normally off LED offers relatively high impedance in OFF state. This potential problem can be eliminated by reducing the LED OFF state impedance. This is accomplished by providing a low impedance shunt path around the LED when it is OFF. Figure 11 illustrates a shunt LED drive circuit.

SHUNT LED DRIVE

To improve noise immunity, a shunt LED drive can be used. The advantages of a shunt LED drive are: 1) it improves CMTI in a half−bridge drive, and 2) the load dv/dt coupling via the package capacitance is coupled into a low−impedance (either the conducting LED or the on resistance of a conducting BJT or logic gate). The disadvantage is that it is the least efficient (e.g., power is consumed when the LED is ON or OFF).

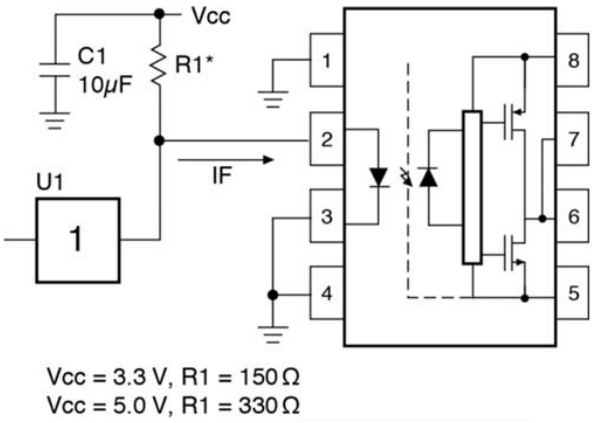

Figure 11. FOD3182 with Shunt LED Drive

When the LED is connected in parallel with the driving switch, this creates a current shunt drive. Figure 11 uses an open−drain logic gate, U1, as the driver:

- The LED current flows when the switch is OFF and U1=HIGH.
- The LED offers low impedance to common mode conducted currents.
- To turn the LED OFF, the gate is forced into LOW state. This reduces the voltage across the LED to a value significantly less than the required forward voltage. It also offers a low impedance, reducing the influence that common mode conducted currents have on the LED operation.

External or self−generated common−mode and normal−mode noise can cause operational malfunction. Minimizing the coupling capacitance between the control logic and power semiconductor greatly reduces a common−mode noise transient transition into a normal−mode noise pulse. Using low and balanced impedances at the driving point improves the noise immunity. Controlling power MOSFETs using galvanic isolated drivers minimizes common−mode noise coupling. The internal shield found in the FOD31xx family of MOSFET drivers maximizes driver CMTI. Using a shunt LED driver maximizes the input network's CMTI, reducing the risk of a common−mode noise pulse transitioning into a normal−mode LED drive signal.

HOW TO CALCULATE MAXIMUM SWITCHING FREQUENCY FOR THE FOD3120 POWER MOSFET / IGBT GATE−DRIVER OPTOCOUPLER

To calculate the maximum switching frequency for the FOD3120, use the variables in Table 1.

Table 1. PERFORMANCE RATINGS

Maximum Junction Temperature	125°C
Thermal Resistance (Emitter), R_{thE}	182 K/W
Thermal Resistance (Detector), R_{thD}	141 K/W
Thermal Resistance (Between Emitter and Detector), R_{thED}	560 K/W
Output IC Power Dissipation at T_A = 25°C	250 mW
Output IC Power Dissipation at T_A = 100°C	210 mW
$I_{CCL} = I_{CCH}$	3.8 mA
$R_{DS(ON)}$	3.5 Ω
$V_{CC} - V_{EE}$	30 V
FQA9N90C_F109	
C_{GS}	2730 pF
ESR C_{GS}	25 Ω

Analysis

The first step in calculating the maximum switching frequency is to determine the maximum power that can be dissipated in the output driver MOSFET of the FOD3120 at a maximum operation junction temperature of 125°C and an ambient temperature of 100°C. The previous section indicates the maximum power at T_A = 100°C is 210 mW based on the steady−state thermal resistance of the FOD3120.

The maximum power in the output IC is the sum of the steady−state IC power and the power dissipated in the output power−MOSFET transistors. The precise relationship is shown in Equation (1):

$$P_{IC} = P_{STATIC} + P_{OUT} \quad \text{(eq. 1)}$$

The static power is:

$$P_{STATIC} = I_{CC} \times V_{CC}$$
$$P_{STATIC} = 3.8\ mA \times 30\ V$$
$$P_{STATIC} = 114\ mW \quad \text{(eq. 2)}$$

The maximum allowable power dissipation in the output transistor, P_{OUT}, is the difference between the maximum IC power, P_{IC}, and the static IC power, P_{STATIC}.

$$P_{OUT} = P_{IC} - P_{STATIC}$$
$$P_{OUT} = 210\ mW - 1140\ mW$$
$$P_{OUT} = 96\ mW \quad \text{(eq. 3)}$$

At an ambient temperature of 100°C, the output transistor can dissipate a steady−state power of 96 mW. The output power is dissipated in the drain−to−source series resistance, $R_{DS(ON)}$, of the output P−channel and N−channel transistors.

The output power equation is given below:

$$P_{OUT} = I_O^2 \times R_{RDS(ON)} \quad \text{(eq. 4)}$$

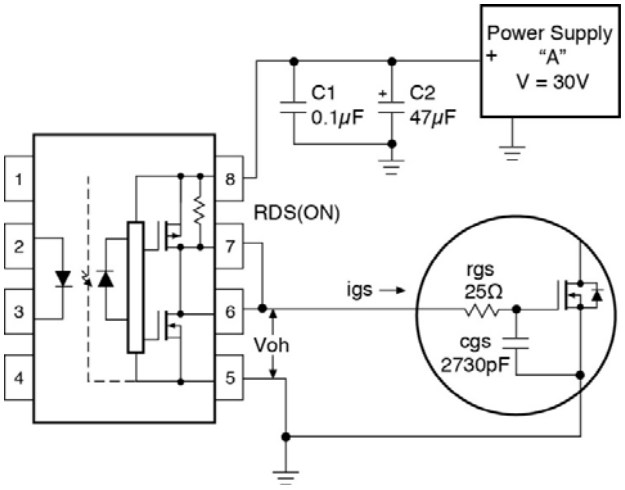

Figure 12. FOD3120 – MOSFET Interface

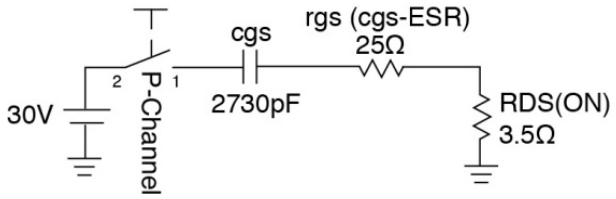

Figure 13. Equivalent Circuit FOD3120 – MOSFET Interface

Figure 12 shows the interconnection between the FOD3120 and an N−channel power MOSFET. Figure 13 provides the equivalent circuit to be used to calculate the FOD3120's output power. The P−channel transistor is modeled as a switch with a series resistance of 3.5 Ω. The input of the FQA9N90C_F109 is modeled as a series RC circuit. The circuit elements are a gate−to−source capacitance of 2730 pF in series with a 25 Ω equivalent capacitor resistance (ESR).

The next section discusses the RMS power dissipated in the output transistors given the charging and discharging current of the MOSFET's gate and the voltage drop across the $R_{DS(ON)}$ of the FOD3120's transistors.

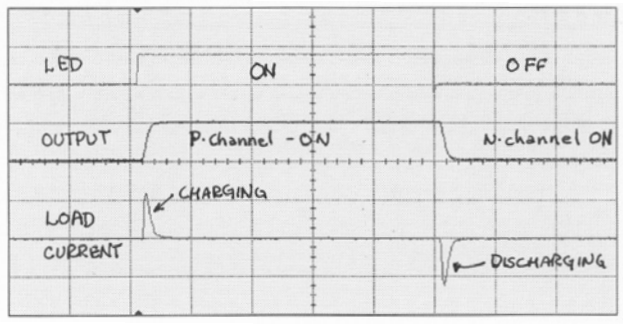

Figure 14. FOD3120 Output Current and Voltage

Figure 14 shows the output current waveform when the FOD3120 is driving the gate of the power MOSFET. Looking again at Figure 13, the initial charging transition is shown as a switch connected to the series of R_{GS}, $R_{DS(ON)}$ and the input capacitance c_{GS}. When the switch is thrown, the current rises up to the peak value of V_{CC}/r_{GS}. The charging current drops at an exponential rate determined by the c_{GS} and the resistors r_{GS} and $R_{DS(ON)}$.

Assumptions:

$t = 2 \times 10^{-9}, 5 \times 10^{-9} \ldots 3 \times 10^{-6}$
$V = 30$ V
$c = 2730 \times 10^{-12}$
$r = 28.5$
Tau = r x c
$Tau = 7.781 \times 10^{-8}$
$a = 10 \times 10^{-6}$

$$i(t) = \frac{V}{r} \cdot \left(e - \frac{t}{\tau}\right) \qquad \text{(eq. 5)}$$

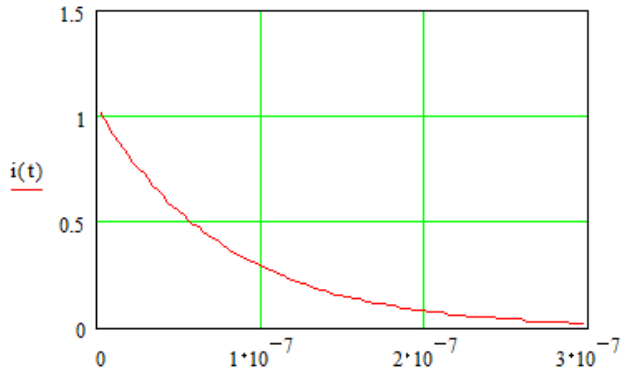

Figure 15. FOD3120 Output Current

The peak power dissipation in the FOD3120's MOSFETs is determined by the peak current and the exponential decay time, t, where:

V = supply voltage;
r = sum of ESR for R_s of the driven MOSFET and $R_{DS(ON)}$ of the FOD3120; and
τ = the time constant of the r and C_{ISS} of the driven MOSFET.

$$Po = \left(\frac{V}{r} \cdot \exp\left(-\frac{t}{\tau}\right)\right)^2 \cdot Rdson \qquad \text{(eq. 6)}$$

The junction rise in the output is a product of the thermal resistance and the output driver's RMS power. The equation for calculating the RMS power is given in Equation (7). The variable, p, is the time period during which the power pulse is averaged. Figure 14 illustrates that a drive current pulse is present at each LED transition. The frequency of operation is defined as 1 / (2 x p). This definition is carried through the balance of the analysis:

$$Po(RMS) = \sqrt{\frac{1}{p} \cdot \int_0^p \left(\frac{V}{r} \cdot \exp\left(-\frac{t}{\tau}\right)\right)^2 \cdot Rdson\, dt} \qquad \text{(eq. 7)}$$

Equation (8) is the elementary calculus solution to the definite integral given in Equation (7), $R_{DS} = R_{DS(ON)}$:

$$Po(RMS) = \frac{V^2 \cdot Rds}{2 \cdot r^2} \cdot \sqrt{\frac{\tau}{p} \cdot \left(1 - \exp\left(\frac{-4 \cdot p}{\tau}\right)\right)} \qquad \text{(eq. 8)}$$

With the aid of Mathcad®, a graphical solution to the equation can be generated.

Assumptions:

$t = 3 \times 10^{-6}, 3.5 \times 10^{-6} \ldots 20 \times 10^{-6}$
$V = 30$ V
$c = 2730 \times 10^{-12}$
$r1 = 25$
$R_{DS} = 3.5$
$R = r1 + R_{DS}$
Tau = r x c

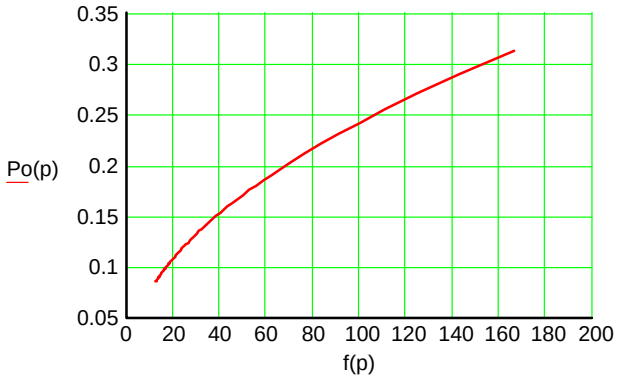

Figure 16. Output Power Dissipation (W) vs. Operations Frequency (kHz)

Figure 16 indicates that the maximum permissible frequency of operation when driving the FQA9N90C_F109 with an output power dissipation of 96 mW is less than 20 kHz. The major limiting factor is the worst−case specification − $R_{DS(ON)}$ of the output drivers.

If the part's maximum $R_{DS(ON)}$ is specified at a value closer to its typical value of 1.0 Ω when operating at an I_O of 1 A, the results shown in Figure 17 are possible.

Assumptions:

V_{CC} = 30 V
C_{gs} = 2730 pF
R_{ds} = 1.0 Ω
r = r1 + $R_{DS(ON)}$
r1 = R_{GS}(c_{GS}−ESR) = 25 Ω

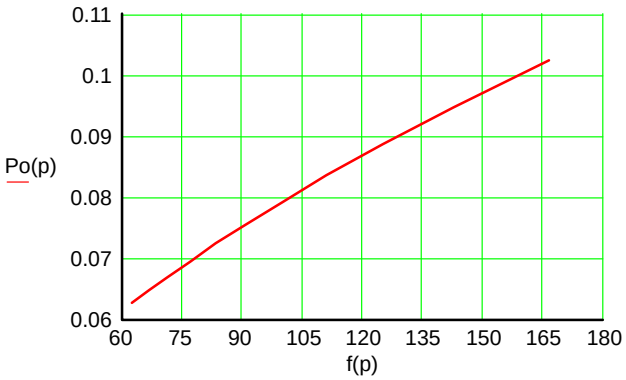

Figure 17. Output Power Dissipation (W) vs. Operation Frequency (kHz)

Figure 17 illustrates that if the $R_{DS(ON)}$ is equal to 1.0 Ω; driving the FQA9N90C_F109 MOSFET at 100°C and V_{CC} = 30 V, a switching frequency of 150 kHz is possible.

CONCLUSION

This application note highlights some of the ways in which the reliability and performance of isolated gate drive circuits can be optimized. The common equations used to calculate the gate charge transfer power apply to the power supplied to the driven MOSFET (FQA9N90C_F109). However, this analysis does not describe the power dissipation within the driver IC. Equation (8) calculates the power dissipated in the FOD3120's output power MOSFETs as a function of $R_{DS(ON)}$, V_{CC}, the driven MOSFET's gate capacitance, and the gate's ESR.

RELATED DATASHEETS

FOD3120 − High Noise Immunity, 2.5 A Output Current, Gate Drive Optocoupler
FOD3182 − 3 A Output Current, High Speed MOSFET Gate Driver Optocoupler
FOD3184 − 3 A Output Current, High Speed MOSFET/IGBT Gate Driver Optocoupler
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